

Docket No. 244789US2 /mtm



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

IN RE APPLICATION OF: Mitsuhiro NOGUCHI, et al.

SERIAL NO: 10/696,028

GAU: 2818

FILED: October 30, 2003

EXAMINER:

FOR: SEMICONDUCTOR MEMORY DEVICE

**INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97**

COMMISSIONER FOR PATENTS  
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

**REFERENCES**

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

**RELATED CASES**

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

**CERTIFICATION**


- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

**DEPOSIT ACCOUNT**

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,  
MAIER & NEUSTADT, P.C.

  
Marvin J. Spivak

Registration No. 24,913

Joseph A. Scafetta, Jr.  
Registration No. 26, 803

Customer Number

**22850**

Tel. (703) 413-3000  
Fax. (703) 413-2220  
(OSMMN 05/03)



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FOR: SEMICONDUCTOR MEMORY DEVICE

**STATEMENT OF RELEVANCY**

**Reference AA (US 6,421,272) on Form PTO 1449:**

This reference shows examples of sense amplifier and redundancy circuits in the NANO-type flash memory.

**Reference AB (US 5,627,786) on Form PTO 1449:**

This reference describes address decoding circuits which access redundancy memory cells with a single timing of data-selection-line voltage application, whereas ours has plural timings of the data-selection-line voltage application to the redundancy memory cells.

**Reference AC (US 6,496,428) on Form PTO 1449:**

This reference describes address decoding circuits which access redundancy memory cells with a single timing of data-selection-line voltage application, whereas ours has plural timings of the data-selection-line voltage application to the redundancy memory cells.

**Reference AD (US 6,269,034) on Form PTO 1449:**

This reference describes address decoding circuits which access redundancy memory cells with a single timing of data-selection-line voltage application, whereas ours has plural timings of the data-selection-line voltage application to the redundancy memory cells.

**Reference AE (US 6,166,973) on Form PTO 1449:**

This reference describes address decoding circuits which access redundancy memory cells with a single timing of data-selection-line voltage application, whereas ours has plural timings of the data-selection-line voltage application to the redundancy memory cells.

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EXAMINER:

SEMICONDUCTOR MEMORY DEVICE

**STATEMENT OF RELEVANCY**

**Reference AO (JP 2000-76880) on Form PTO 1449:**

This reference shows a wiring layout of data selection lines in the NANO – type flash memory.

**Reference AP (JP 2001-167592) on Form PTO 1449:**

This reference shows examples of sense amplifier and redundancy circuits in the NANO-type flash memory.

**Reference AQ (JP 2000-021190) on Form PTO 1449:**

This reference shows examples of sense amplifier and redundancy circuits in the NANO-type flash memory.

**Reference AR (JP 2002-150783) on Form PTO 1449:**

This reference shows a circuit diagram of the NANO – type flash memory.

**Reference AV (JP 2001-67894) on Form PTO 1449:**

This reference describes address decoding circuits which access redundancy memory cells with a single timing of data-selection-line voltage application, whereas ours has plural timings of the data-selection-line voltage application to the redundancy memory cells.



SHEET 1 OF 1

Form PTO 1449 (Modified)		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO. 244789US2		SERIAL NO. 10/696,028	
LIST OF REFERENCES CITED BY APPLICANT				APPLICANT Mitsuhiro NOGUCHI, et al.			
				FILING DATE October 30, 2003		GROUP 2818	
U.S. PATENT DOCUMENTS							
EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	6,421,272	07/16/2002	M. NOGUCHI			
	AB	5,627,786	05/06/1997	F. F. ROOHPARVAR			
	AC	6,496,428	12/17/2002	C. OHNO, et al.			
	AD	6,269,034	07/31/2001	M. SHIBUYA			
	AE	6,166,973	12/26/2000	N. SHINOZAKI			
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						
FOREIGN PATENT DOCUMENTS							
		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION YES NO		
	AO	2000-76880	03/14/2000	JAPAN (with English Abstract)			X
	AP	2001-167592	06/22/2001	JAPAN (with English Abstract)			X
	AQ	2000-021190	01/21/2000	JAPAN (with English Abstract)			X
	AR	2002-150783	05/24/2002	JAPAN (with English Abstract)			X
	AS	2001-176290	06/29/2001	JAPAN (with English Abstract)			X
	AT	2002-216470	08/02/2002	JAPAN (with English Abstract)			X
	AU	2000-357395	12/26/2000	JAPAN (with English Abstract)			X
	AV	2001-067894	03/16/2001	JAPAN (with English Abstract)			X
	AW						
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)							
	AX						
	AY						
	AZ						
					<input type="checkbox"/> Additional References sheet(s) attached		
Examiner					Date Considered		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							